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PENDING CLAIMS:

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

- 1. (withdrawn) A method of forming a conductive structure within an integrated circuit 1 comprising: 2 forming a conformal tungsten layer over a dielectric layer and within openings within 3 the dielectric layer; 4 forming a protective barrier layer over the tungsten layer, wherein the protective barrier 5 layer comprises a material for which removal by chemical mechanical polishing is primarily 6 7 mechanical; and 8 removing at least portions of the protective barrier layer and the tungsten layer by
- 2. (withdrawn) The method as set forth in Claim 1 wherein the step of forming a protective 1 barrier layer over the tungsten layer further comprises: 2
- forming a titanium or titanium nitride layer on the tungsten layer. 3

chemical mechanical polishing.

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- 3. (withdrawn) The method as set forth in Claim 2 wherein the step of removing at least 1 portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing 2 further comprises: 3
- removing portions of the tungsten layer overlying the dielectric layer without removing 4 portions of the tungsten layer within the openings within the dielectric layer. 5
- 4. (withdrawn) The method as set forth in Claim 3 wherein the step of removing at least 1 portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing 2 further comprises: 3
- removing all of the protective barrier layer. 4
- 5. (withdrawn) The method as set forth in Claim 3 wherein the step of removing at least 1 portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing 2 3 further comprises:
- removing portions of the protective barrier layer overlying dielectric regions between 4 the openings within the dielectric layer. 5

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the dielectric layer.

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1	6. (withdrawn) The method as set forth in Claim 5 wherein the step of removing at least
2	portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing
3	further comprises:
4	after removing portions of the protective barrier layer overlying the dielectric regions
5	between the openings within the dielectric layer, removing portions of the tungsten layer
6	overlying the dielectric regions between the openings within the dielectric layer; and
7	during removal of portions of the tungsten layer overlying the dielectric regions between
8	the openings within the dielectric layer, removing portions of the protective barrier layer
9	overlying the openings within the dielectric layer.
1	7. (withdrawn) The method as set forth in Claim 2 wherein the step of removing at least
2	portions of the protective barrier layer and the tungsten layer by chemical mechanical polishing
3	further comprises:
4	removing portions of the protective barrier layer and the tungsten layer overlying
5	dielectric regions between the openings within the dielectric layer to planarize remaining
6	portions of the tungsten layer and remaining portions of the protective barrier layer, if any, with

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8. (previously amended) A portion of an integrated circuit structure comprising: 1 a dielectric layer over a substrate; 2 a conformal tungsten layer over the dielectric layer and within openings within the 3 dielectric layer; and 4 a protective barrier layer over the tungsten layer and within the openings, wherein the 5 protective barrier layer comprises a material for which removal by chemical mechanical 6 polishing is primarily mechanical. 7 9. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1 wherein the protective barrier layer is titanium or titanium nitride. 2 10. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1 wherein portions of the tungsten layer within the openings are thicker than portions of the 2 3 tungsten layer over the dielectric layer. 11. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1 wherein the protective barrier layer overlies the entire tungsten layer. 2

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- 12. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1
- wherein the protective barrier layer overlies portions of the tungsten layer within the openings 2
- but not portions of the tungsten layer over the dielectric layer. 3

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- 13. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1
- wherein the tungsten layer has a thickness of between about 4500 and 8000 angstroms. 2
- 14. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1
- wherein the protective barrier layer has a thickness of between about 100 and 800 angstroms. 2
- 15. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 8 1
- wherein at least one opening within the dielectric layer is sized to form a capacitive electrode 2
- 3 from tungsten within the at least one opening.

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16. (previously amended) A portion of an integrated circuit structure comprising: 1 a dielectric layer having an opening therein; 2 tungsten within the opening; and 3 a portion of a protective barrier layer over a central region of the tungsten and within the 4 opening, wherein the portion of the protective barrier layer comprises a material for which 5 removal by chemical mechanical polishing is primarily mechanical. 6 17. (currently amended) The portion of an integrated circuit structure as set forth in Claim 16 1 wherein an upper surface of the tungsten is exposed around the portion of the protective barrier 2 3 layer. 18. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 16 1 wherein the portion of the protective barrier layer is titanium or titanium nitride. 2 19. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 16 1

wherein the tungsten and the portion of the protective barrier layer form an upper surface which

is substantially planar with an upper surface of the dielectric layer.

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- 20. (unchanged/original) The portion of an integrated circuit structure as set forth in Claim 16
- wherein the opening within the dielectric layer is sized to form a capacitive electrode from the
- 3 tungsten within the opening.